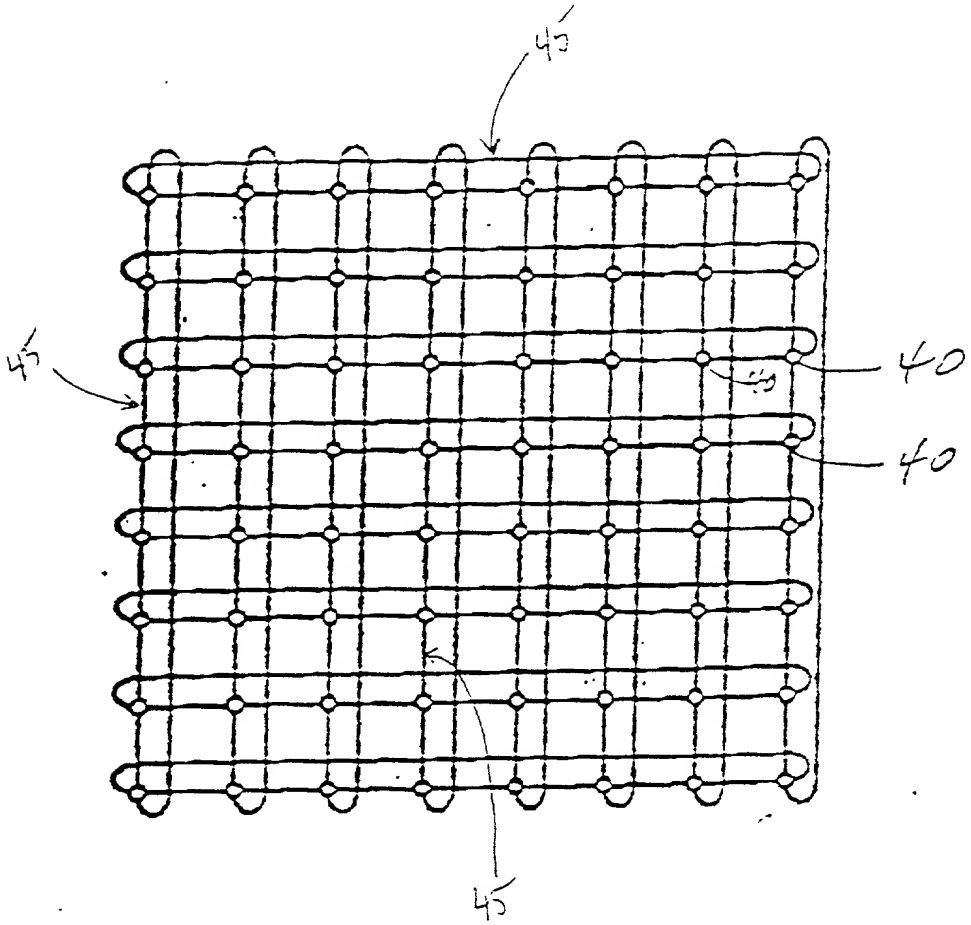


FIG. 1

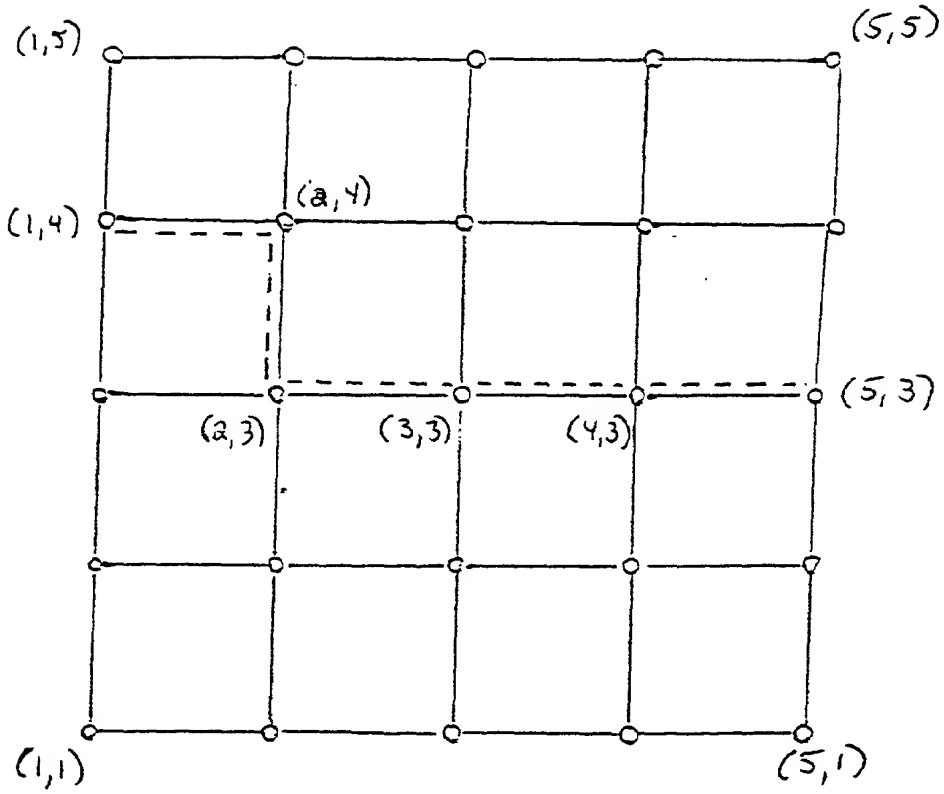


FIG. 2

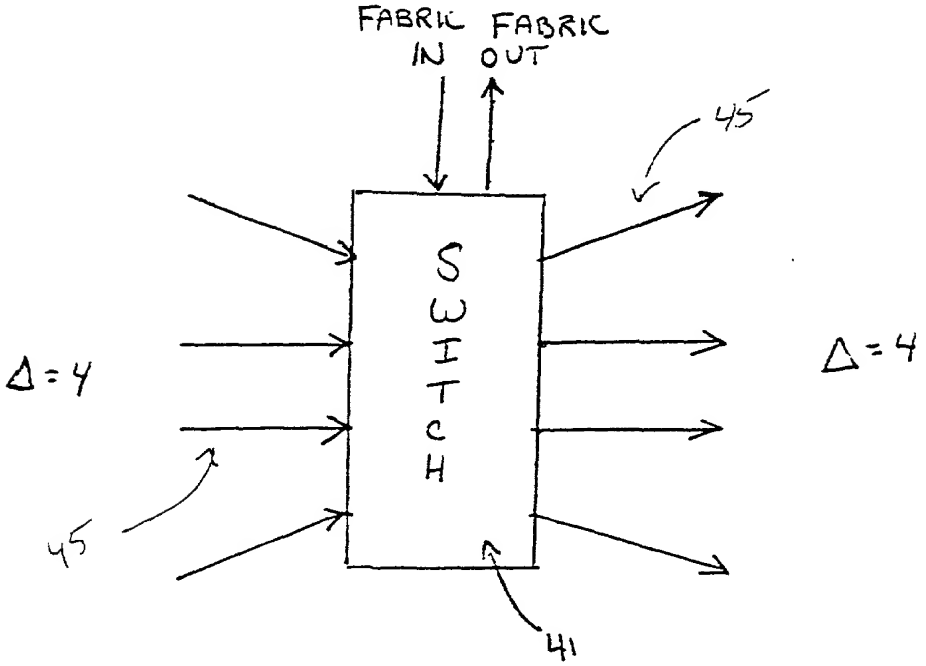


FIG. 3

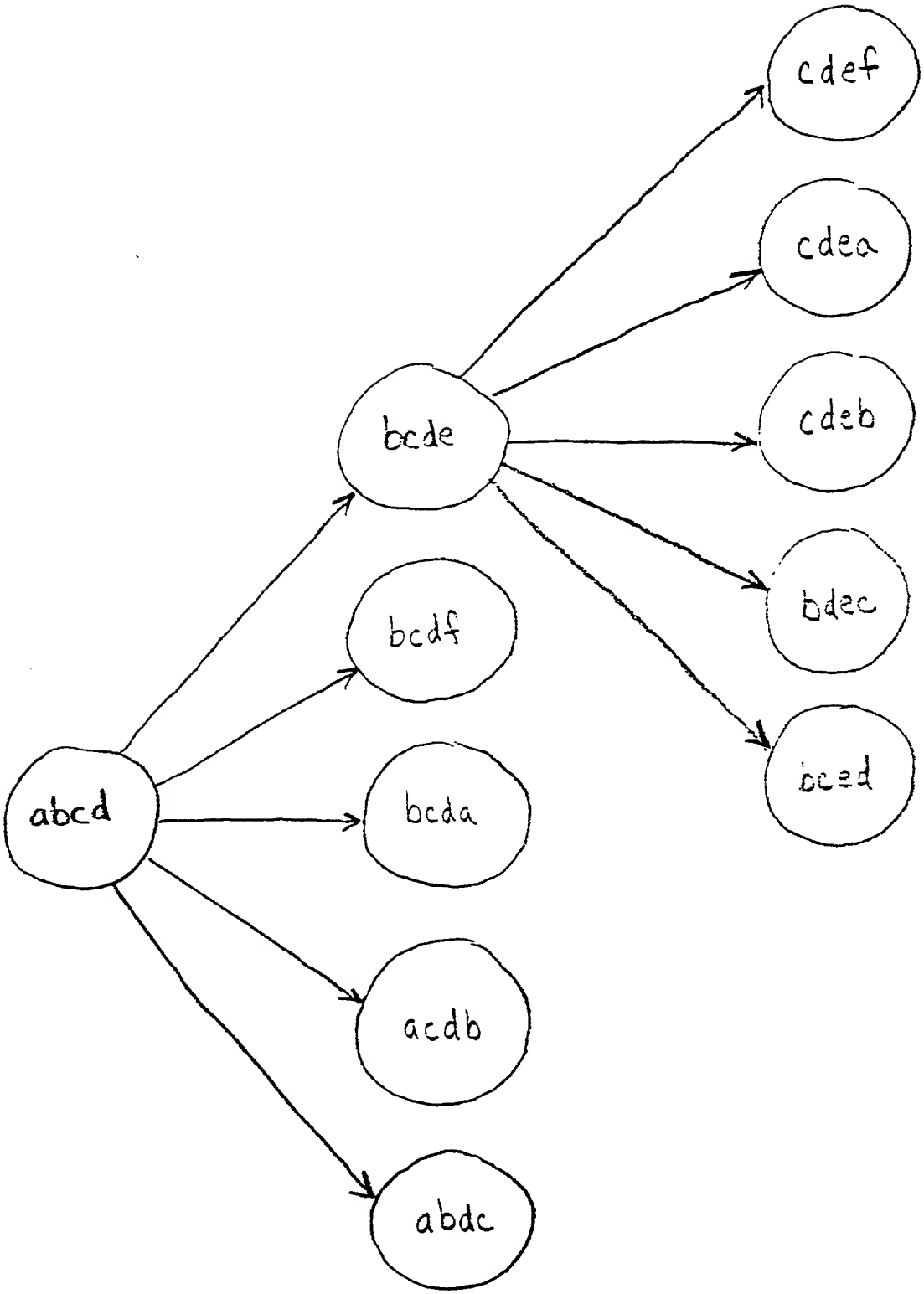


FIG. 4A

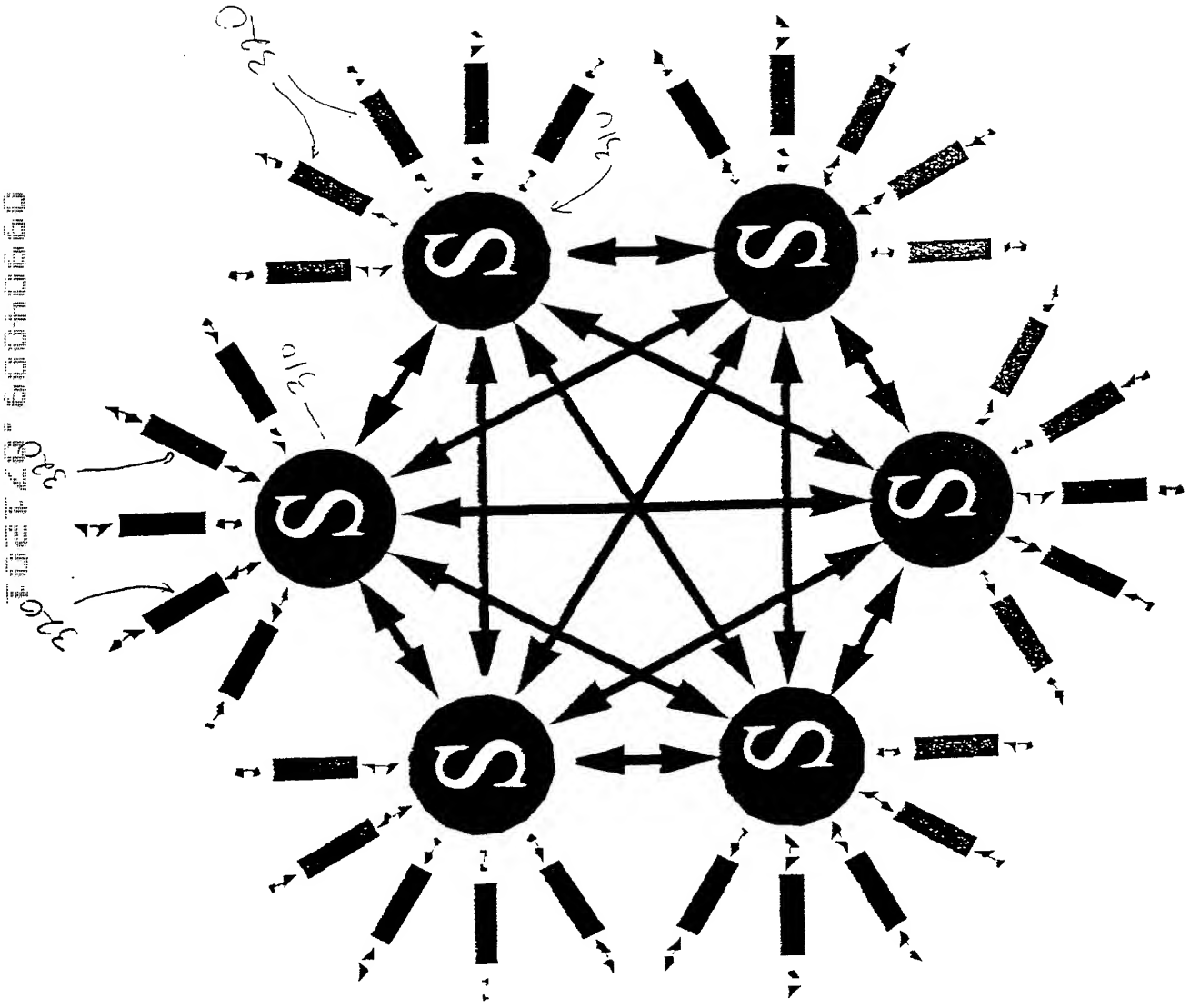


FIG. 4B

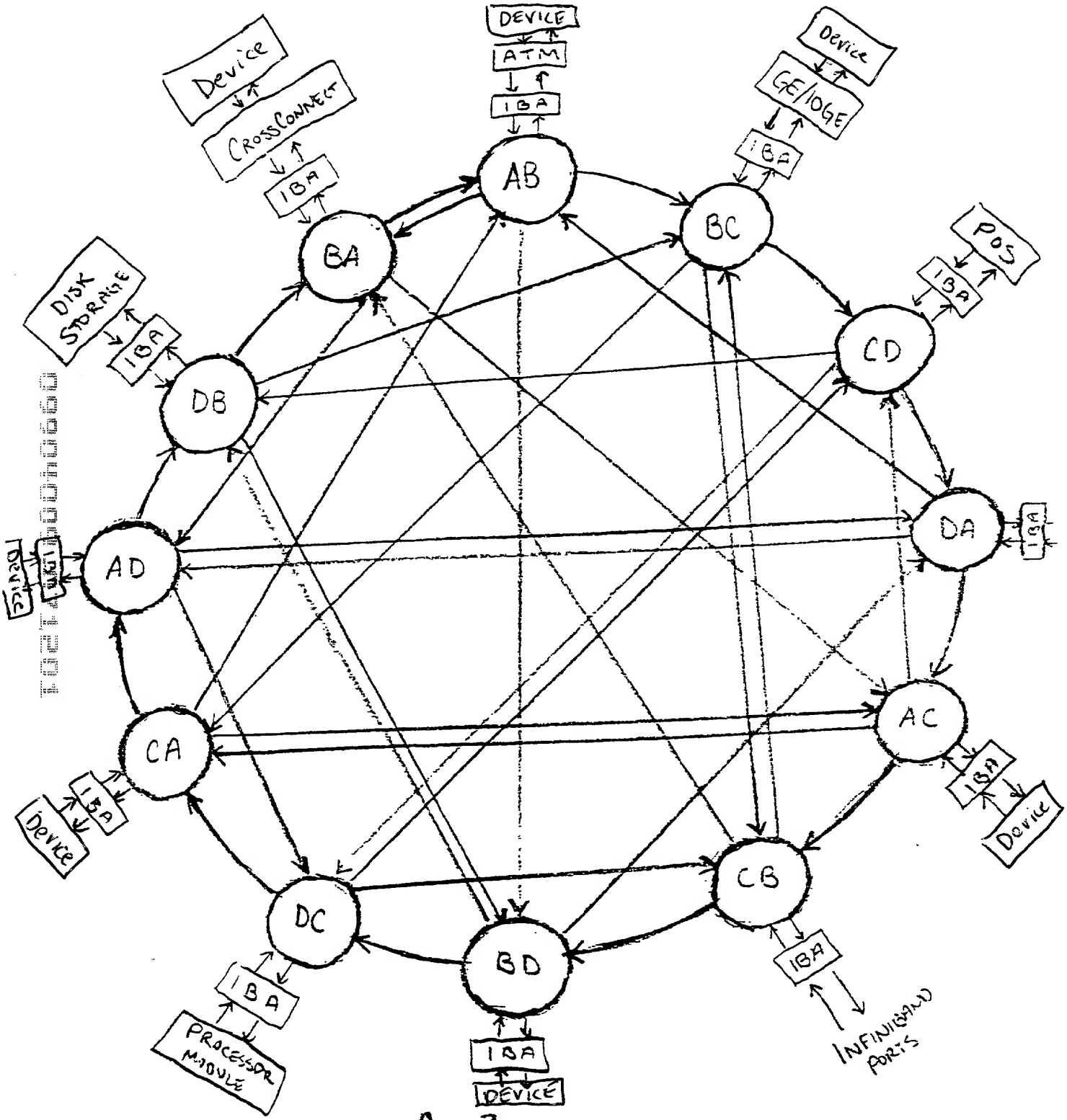

DEVICE
ATM
IBA
AB
Device
CrossConnect
IBA
BA
Device
GE/10GE
IBA
BC
DISK STORAGE
IBA
DB
POS
IBA
CD
Device
IBA
AD
DA
IBA
CA
Device
IBA
AC
IBA
Device
DC
CB
IBA
PROCESSOR MODULE
BD
IBA
INFINIBAND PORTS
IBA
DEVICE
Δ = 3
D = 2

FIG. 5A

ADJACENCY TABLES FOR NODES IN FIG. 5A

AB	**AC**	**AD**
AB → BC	AC → CB	AD → DB
AB → BD	AC → CD	AD → DC
AB → BA	AC → CA	AD → DA
BA	**BC**	**BD**
BA → AC	BC → CD	BD → DA
BA → AD	BC → CA	BD → DC
BA → AB	BC → CB	BD → DB
CA	**CB**	**CD**
CA → AB	CB → BD	CD → DA
CA → AD	CB → BA	CD → DB
CA → AC	CB → BC	CD → DC
DA	**DB**	**DC**
DA →AB	DB → BA	DC → CA
DA →AC	DB → BC	DC → CB
DA →AD	DB → BD	DC → CD

FIG. 5B

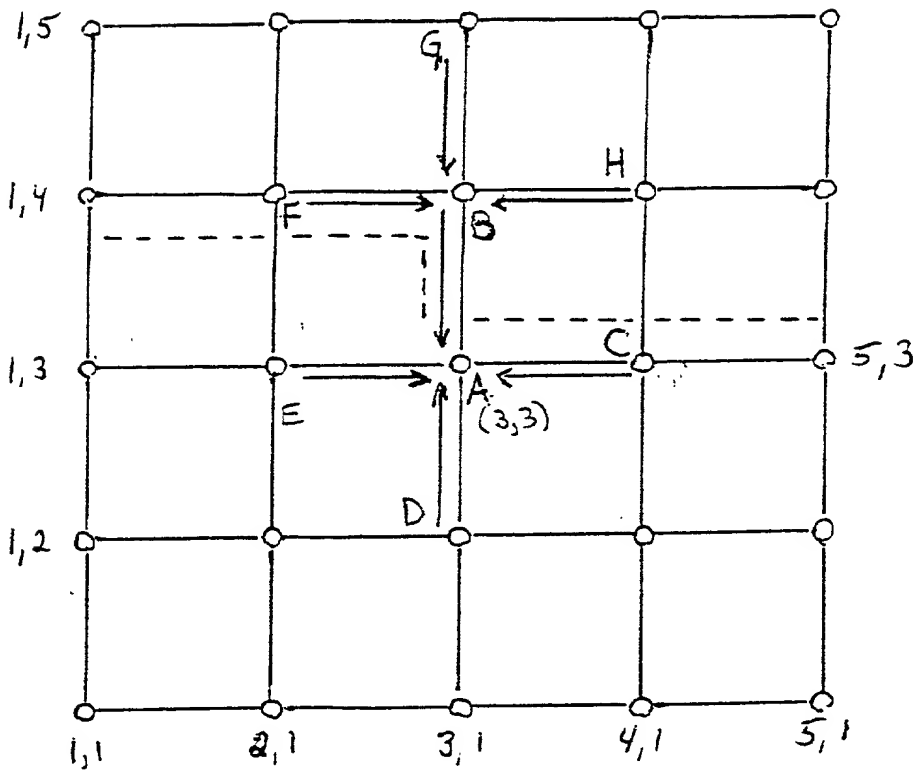
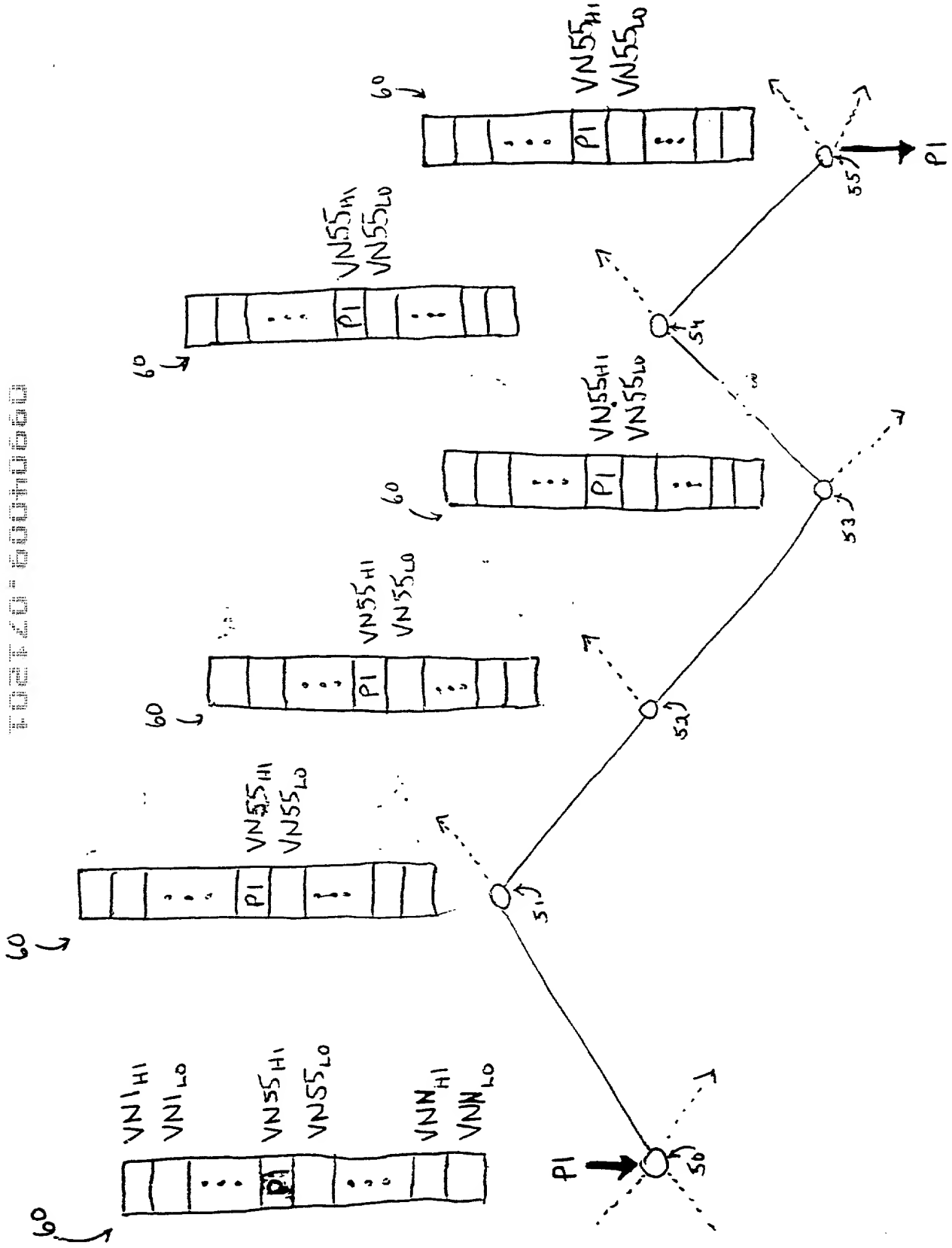


FIG. 6



PRIOR ART

FIG. 7

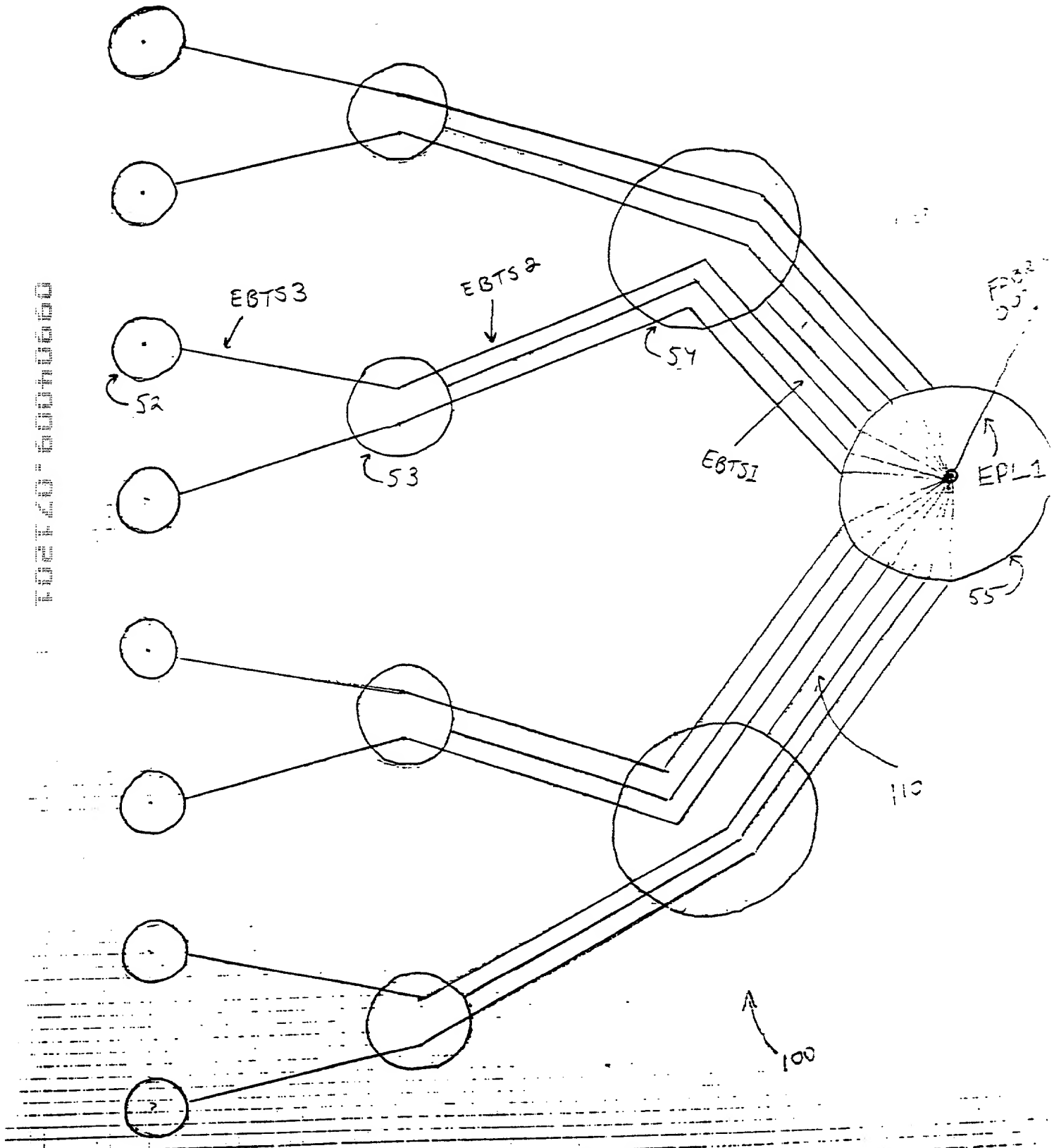


FIG. 8A

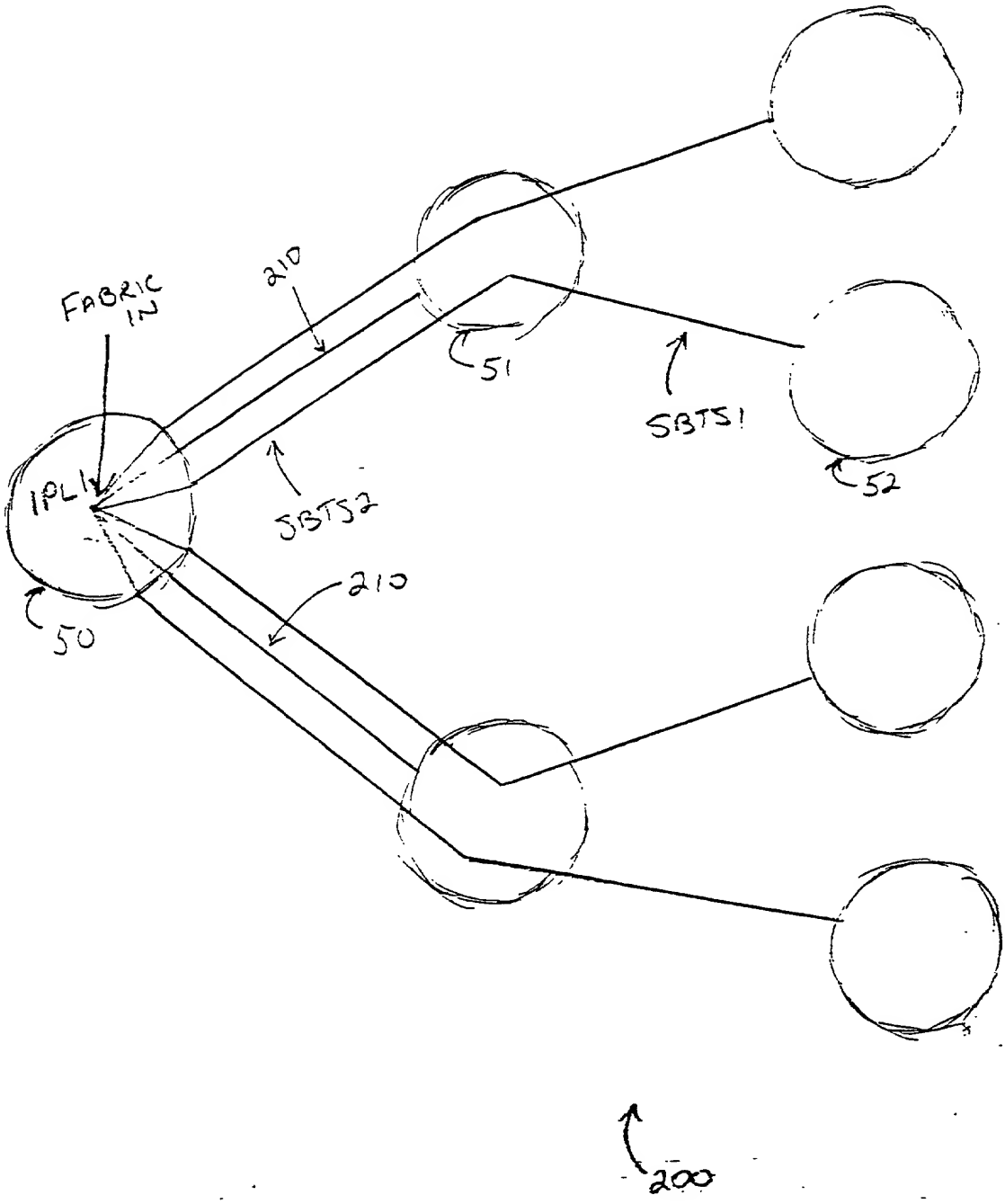


FIG. 8B

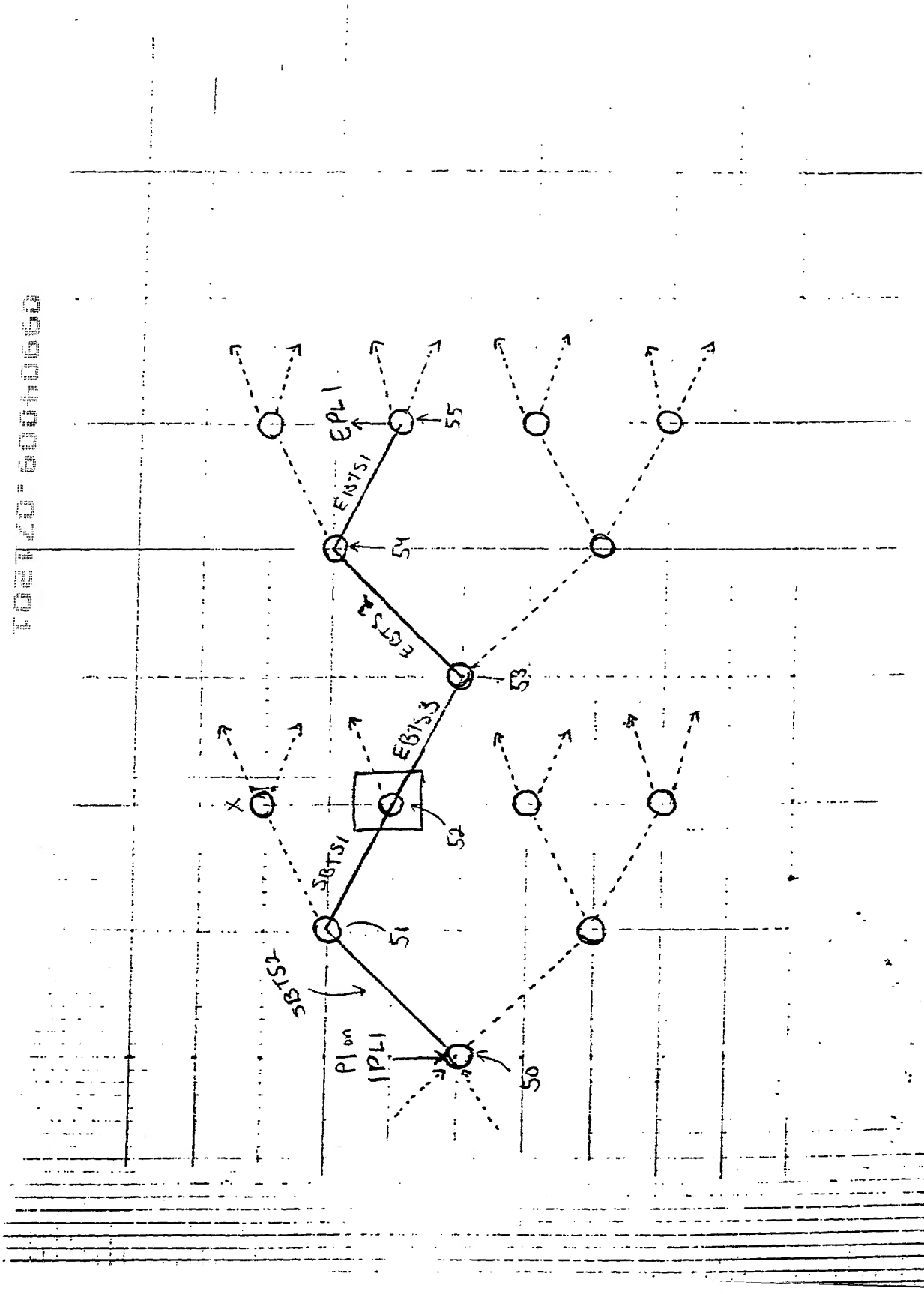

EPL1
55
EBTS1
54
EBTS2
53
EBTS3
52
SBTS1
51
SBTS2
PI on IPL1
50
X

FIG. 9

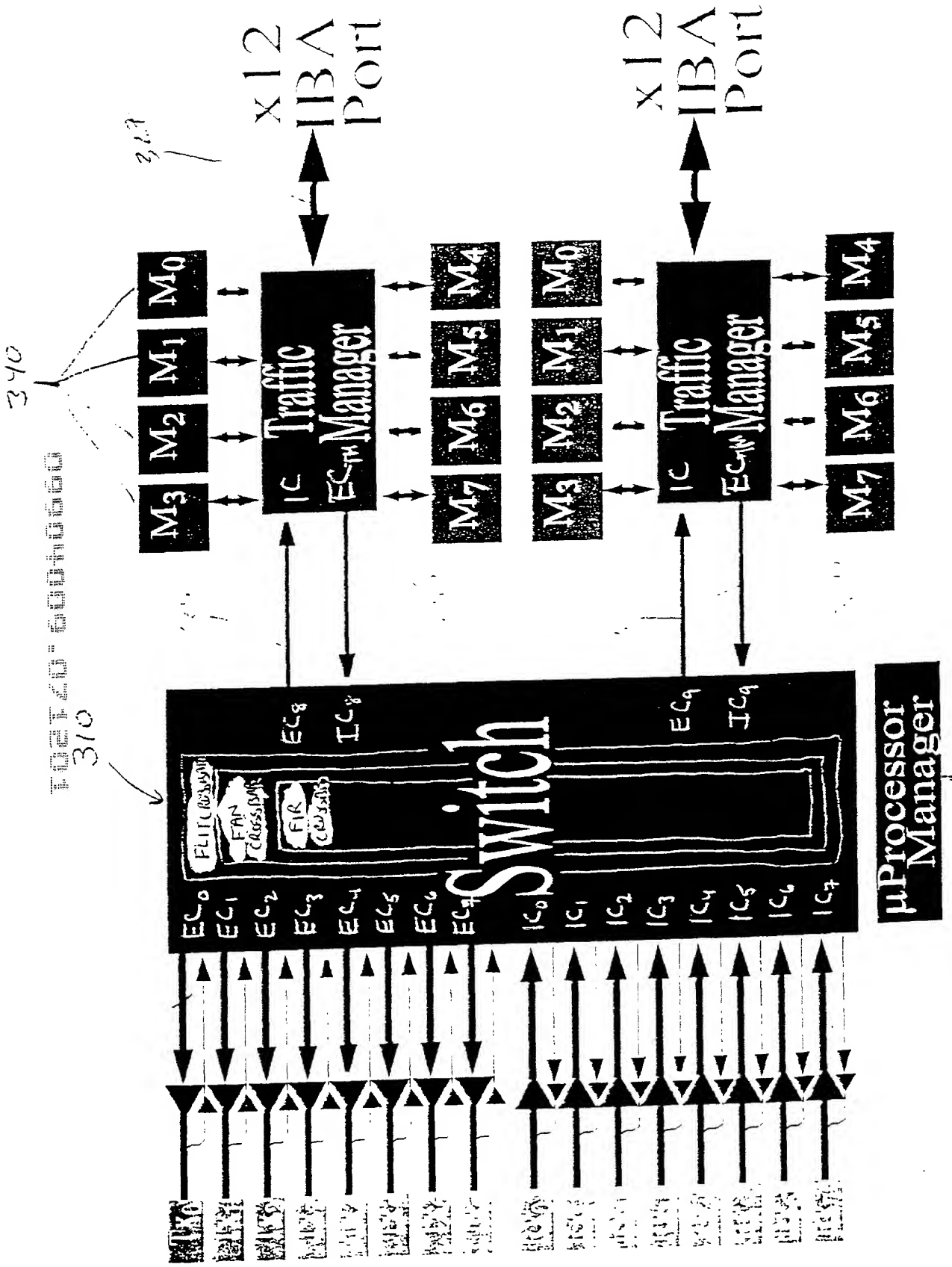

x12 IBA Port
x12 IBA Port
M0
M1
M2
M3
M4
M5
M6
M7
Traffic Manager
Switch
µProcessor Manager
310
320
330
340

FIG. 10

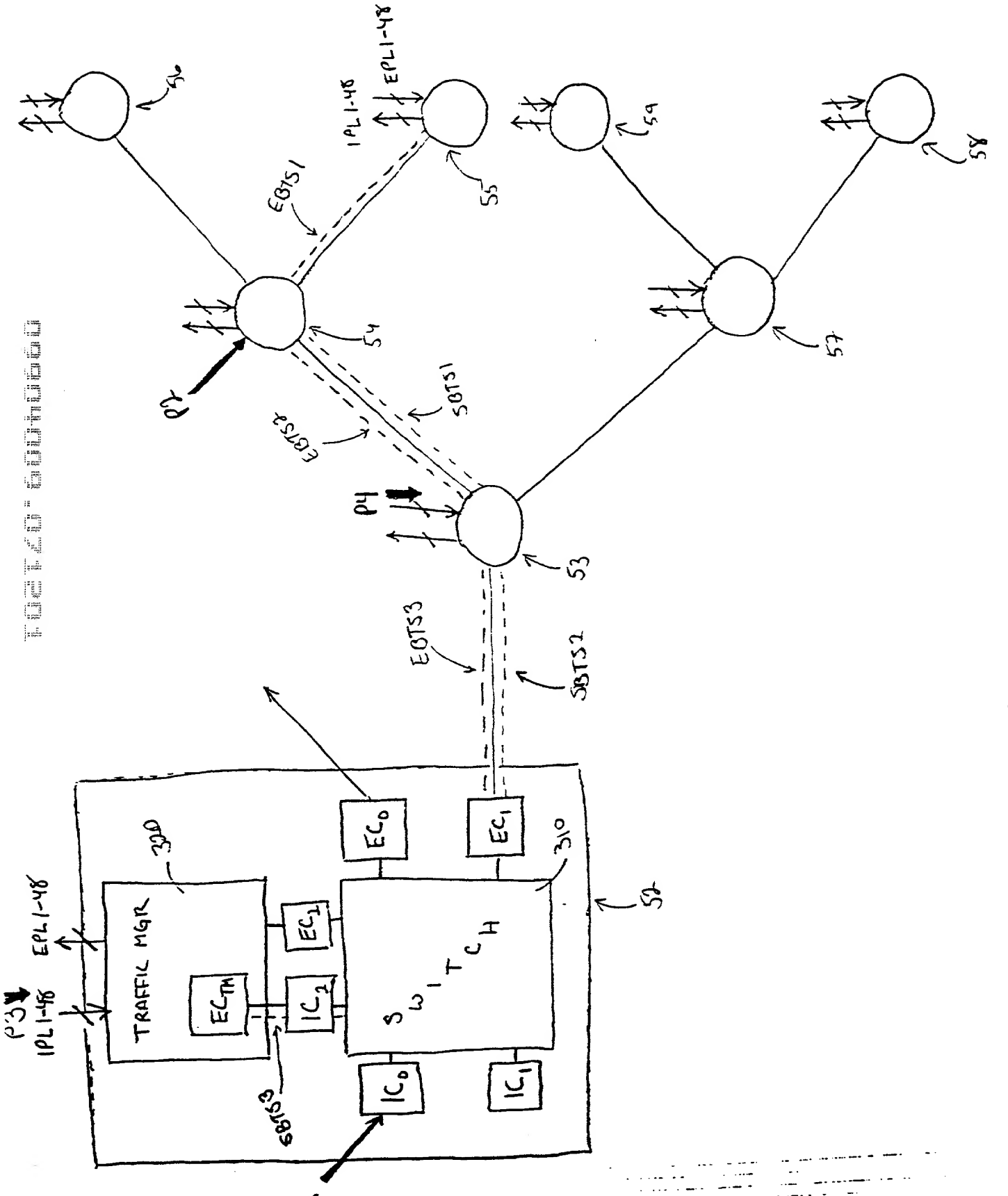

52
EPL1-48
IPL1-48
EOTS1
55
54
59
58
57
P4
SOTS1
EOTS2
P3
53
EOTS3
SOTS2
EC0
EC1
310
52
300
TRAFFIC MGR
EPL1-48
IPL1-48
EC1
EC2
ECTM
SWITCH
IC0
IC1
SOTS3
P1

FIG. 11A

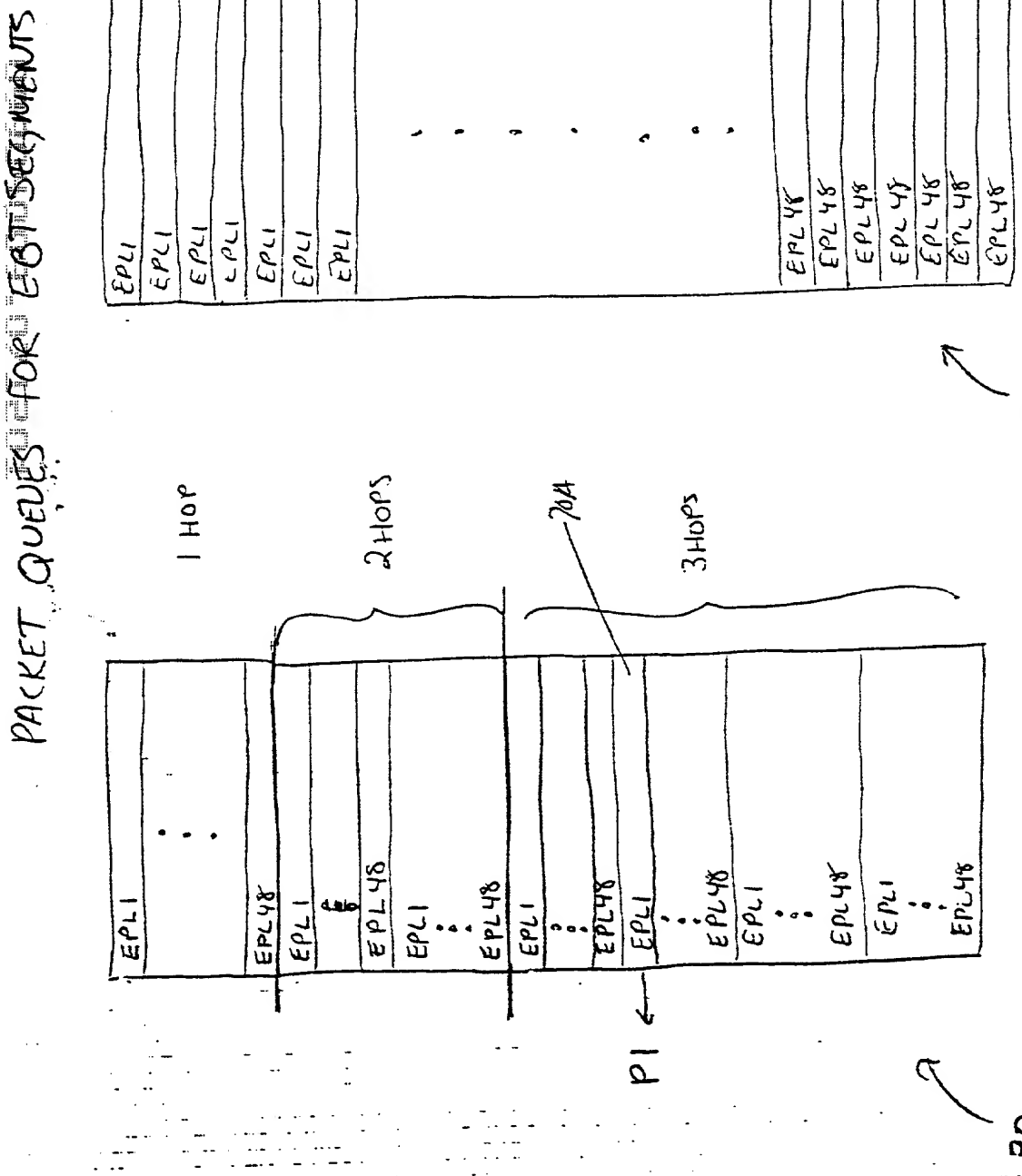


FIG. 11A

FIG. 11C

PACKET QUEUES FOR SIST SEGMENTS

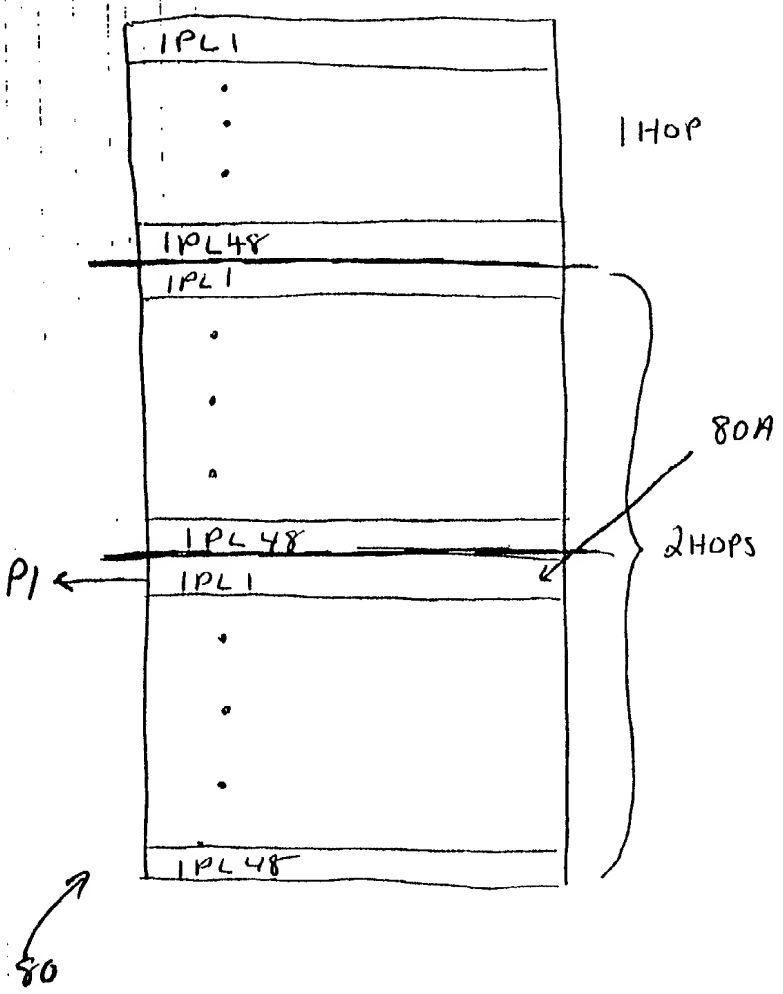


FIG. 11D

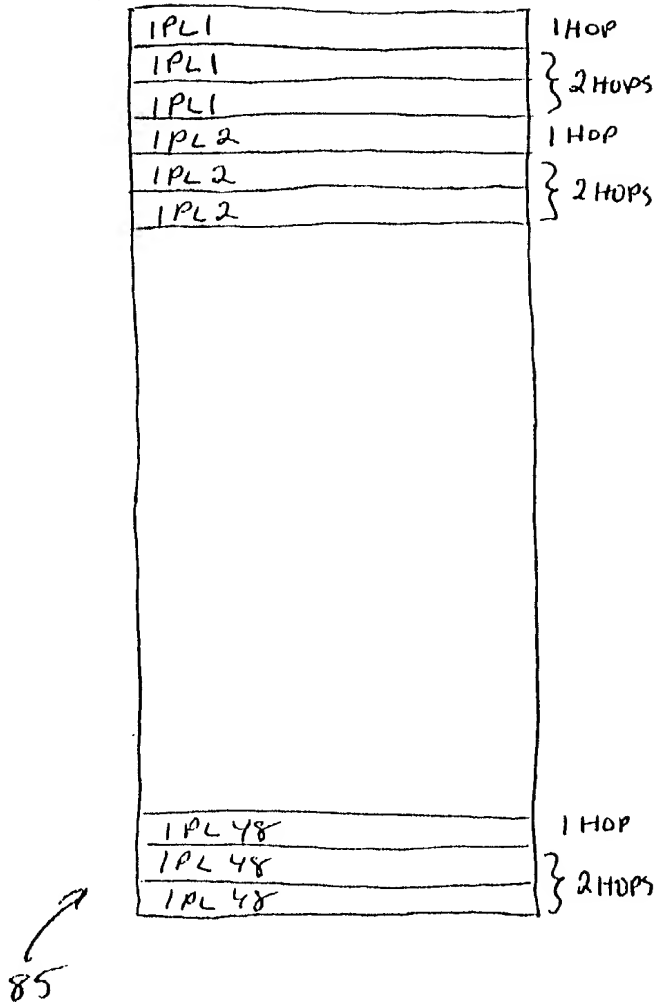


FIG. 11E

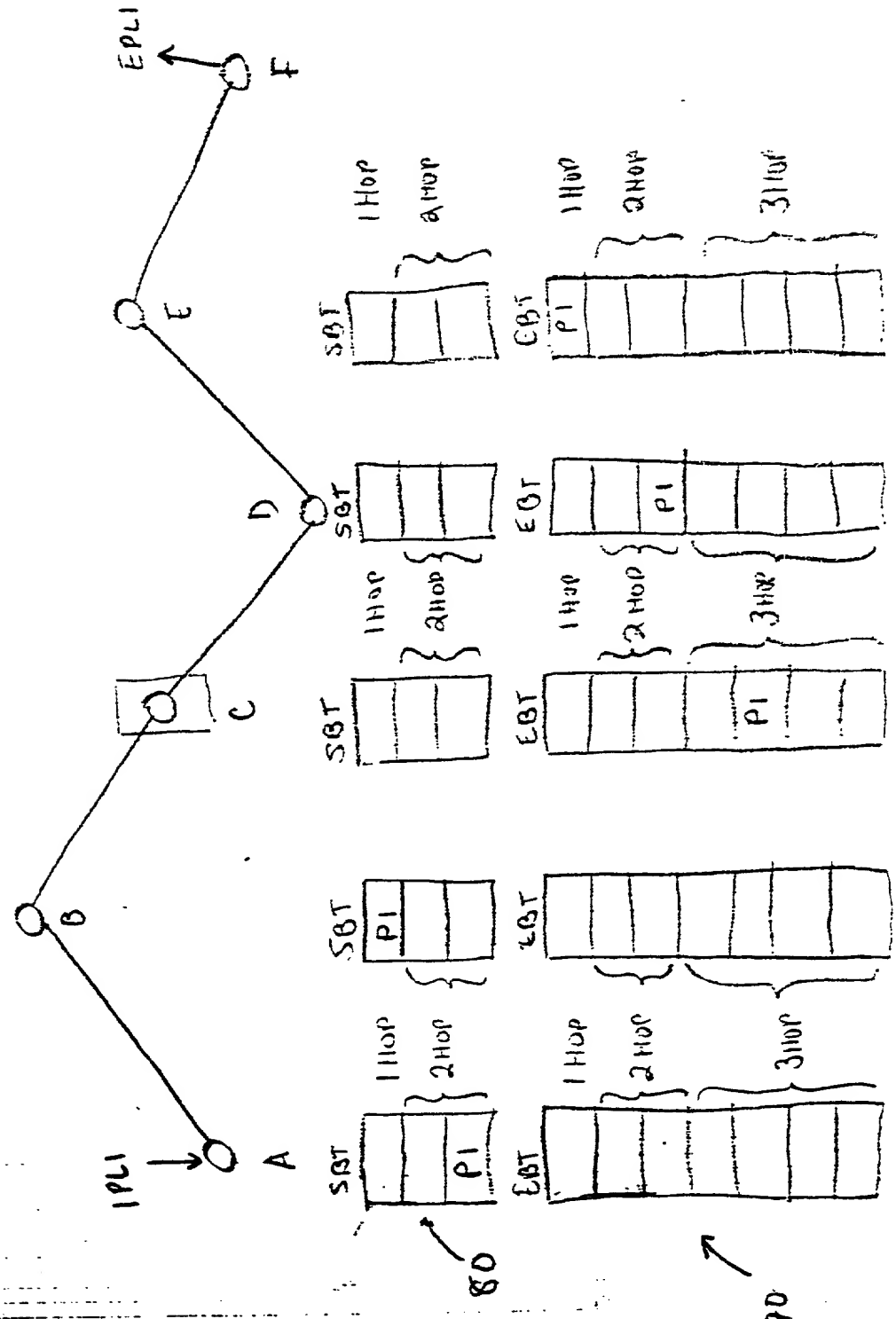


FIG 11F - continued

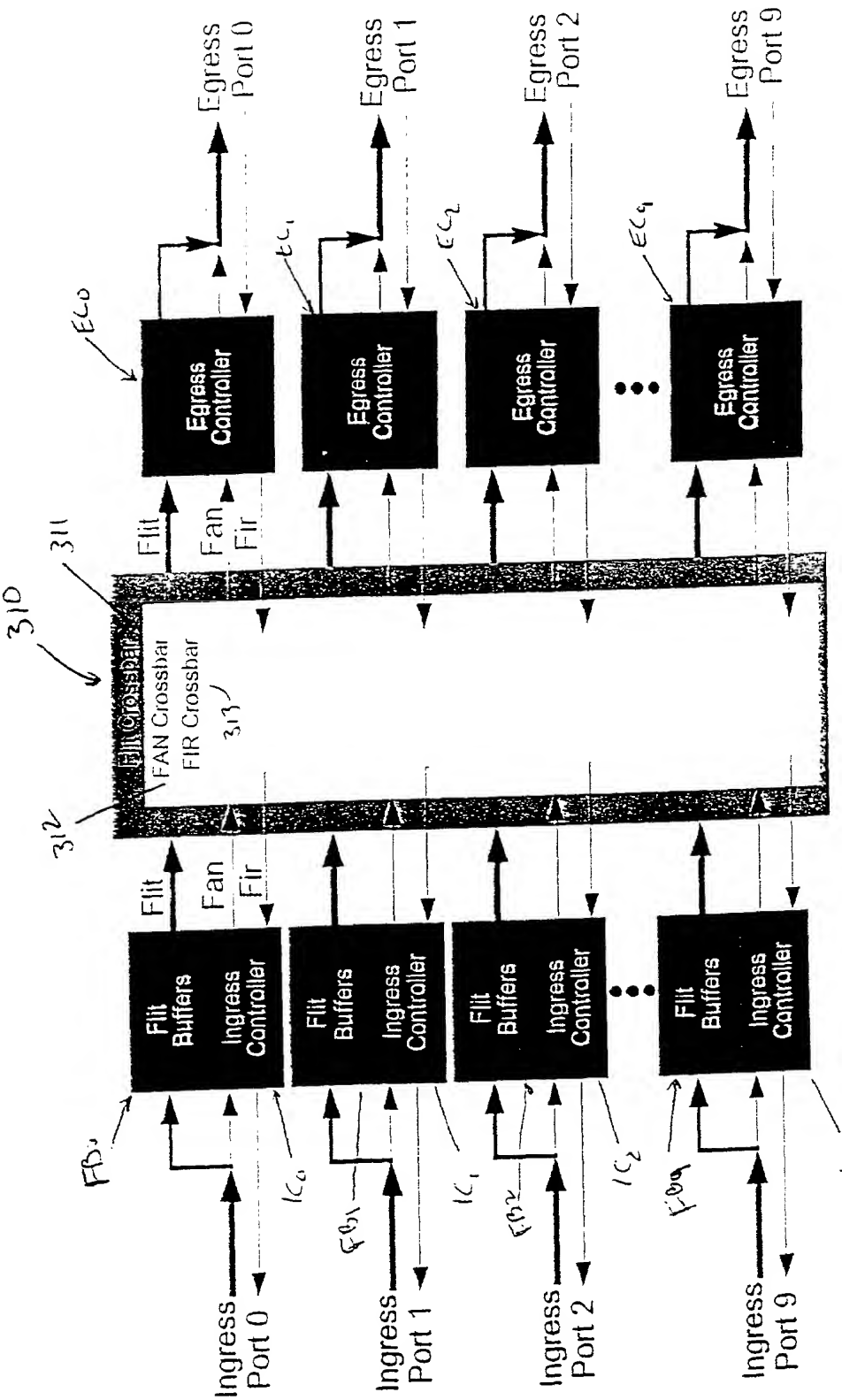

Egress Port 0
Egress Port 1
Egress Port 2
Egress Port 9
Egress Controller
EC0
EC1
EC2
EC9
310
311
312
313
Flit
Fan
Fir
FIR Crossbar
FAN Crossbar
FIR Crossbar
Flit Buffers
Ingress Controller
FB0
FB1
FB2
FB9
IC0
IC1
IC2
IC9
Ingress Port 0
Ingress Port 1
Ingress Port 2
Ingress Port 9

Fig. 12

CONTROL STRUCTURE	SIZE (IN BITS)	DESCRIPTION
IngressPacketState	1280x35=44,800	Each IngressPacketState structure manages the storage of a partially received packet on one of the ingress ports.
EgressLaneState	(128x30=3,480)	Each EgresslaneState structure supplies information used to process received Credits.
AvailableEgressLane	(128x1)	Each flag indicates that a particular lane is available or in use.
FanState	(512x44=22,528)	Each FanState structure holds one FAN waiting to be converted into a FIR and pointers which allow creating a linked list of packets waiting on a particular channel and a linked list of FANs comprising a particular packet.
AvailableFanState	(512x1)	Each flag indicates that a particular local FanState structure is availably or in use.
WaitingForlanes	(2928x1)	Each flag indicates that a particular runnel segment has a packet ready to be assigned to a lane as soon as one becomes available.
WaitingForFSM	(2928x1)	Each flag indicates that a particular channel has a FAN ready to be converted into a FIR as soon as the EgressController has bandwidth available to perform the conversion.
WaitingForFirFifo	(2304x1)	Each flag indicates that a particular lane has a FAN ready to convert into a FIR as soon as room in the FIR FIFO becomes non-full.
SegmentPointer	(2938x13=38,194)	Each SegmentPointer points to a a queue of packets waiting on a runnel segment.

FIG. 13

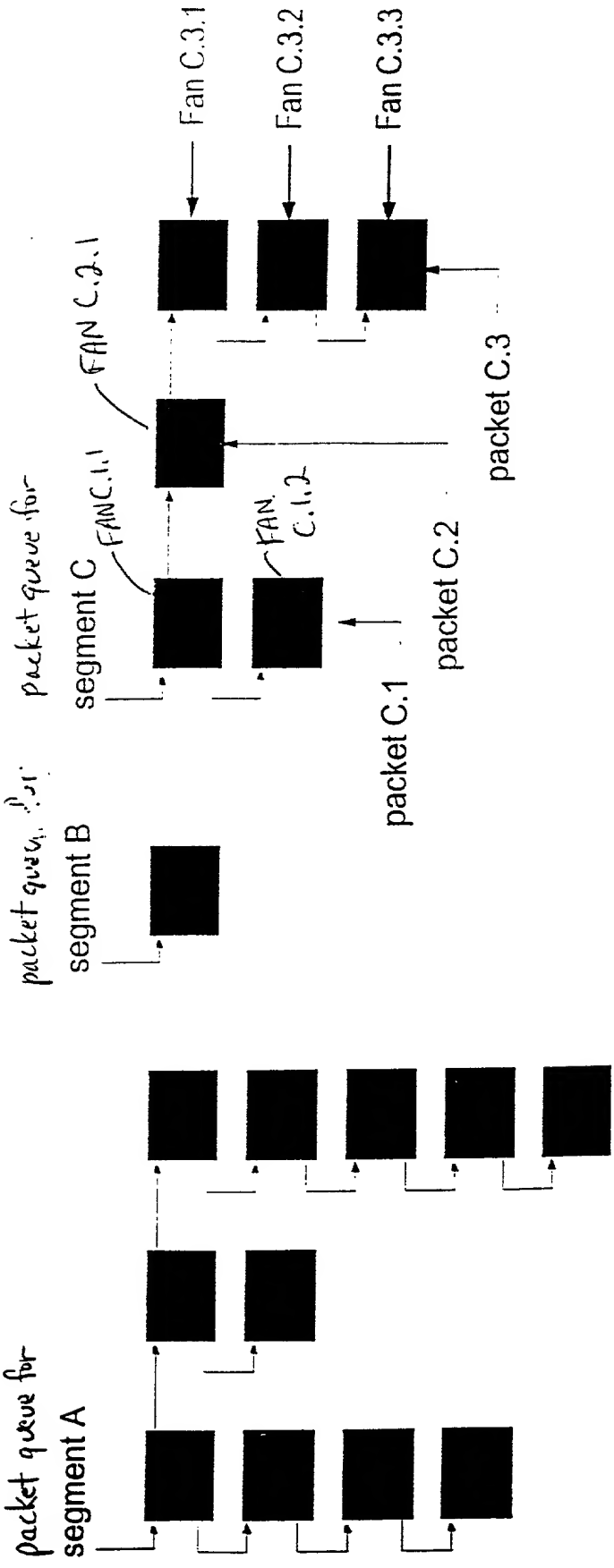

packet queue for segment A
packet queue for segment B
packet queue for segment C
FAN C.1.1
FAN C.1.2
FAN C.2.1
Fan C.3.1
Fan C.3.2
Fan C.3.3
packet C.1
packet C.2
packet C.3

FIG. 14

400
410
420
430
440
450
460
470
480
490
Credit
segment Queue Memory 2938x13
Waiting State Memory 123x456
FAN Selector
Packet State Memory 123x456
FAN Processor
Credit Processo
Flit State Memory 123x456
lane State Memory 123x456
FIR Generator
FirFifo Processo
FanFifo0
FanFifo1
FanFifo2
FanFifo3
FanFifo4
FanFifo5
FanFifo6
FanFifo7
FanFifo8
FanFifo9
FirFifo0
FirFifo1
FirFifo2
FirFifo3
FirFifo4
FirFifo5
FirFifo6
FirFifo7
FirFifo8
FirFifo9

Fig. 15